Fig. 1

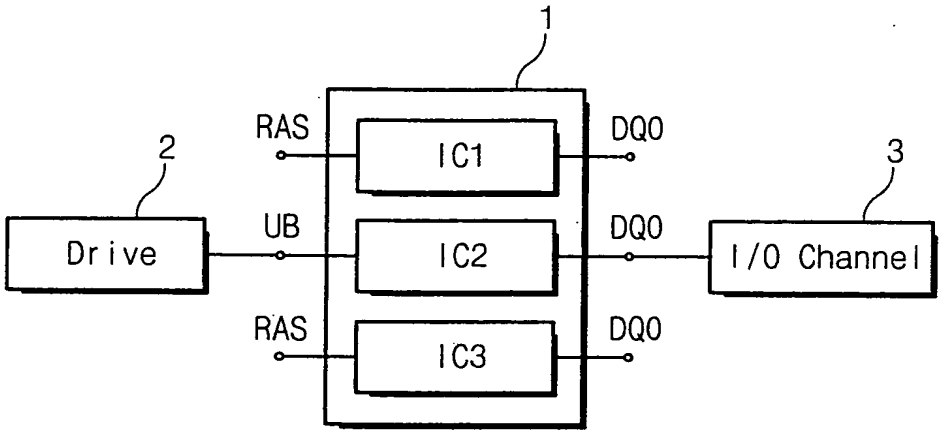

1
2
3
RAS
UB
RAS
IC1
IC2
IC3
DQ0
DQ0
DQ0
Drive
I/O Channel

Fig. 2

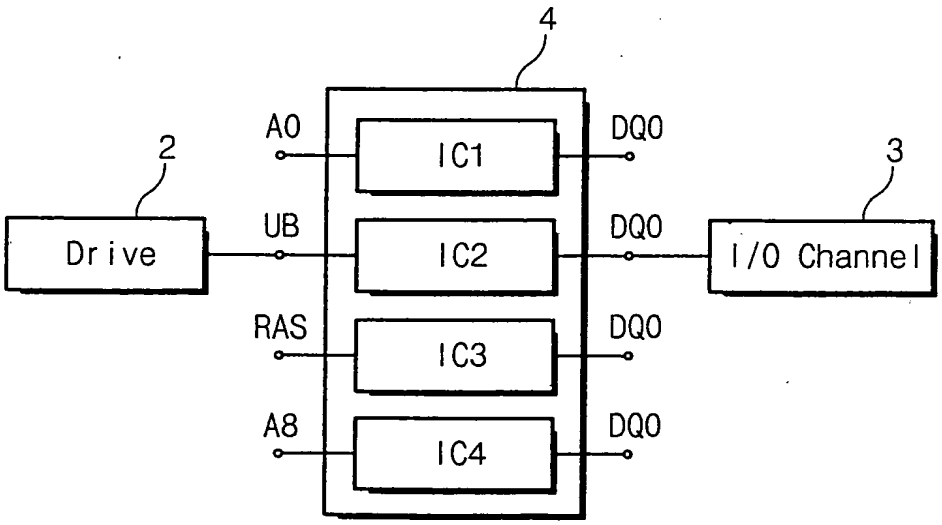
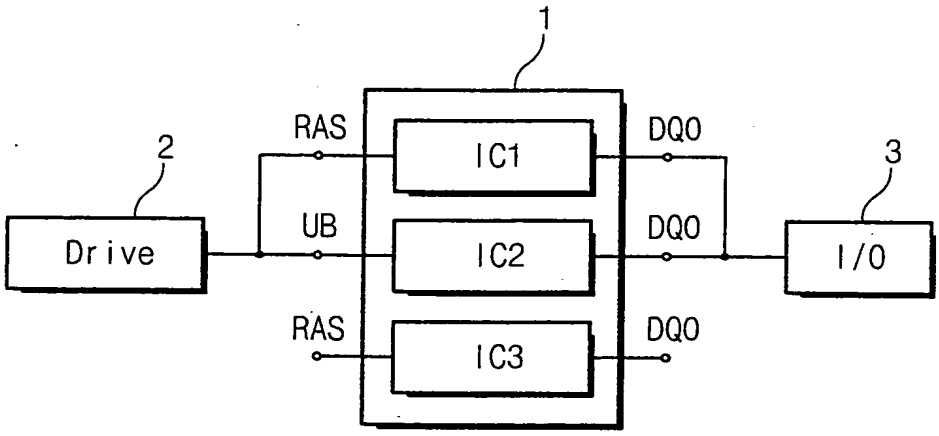

4
2
3
A0
UB
RAS
A8
IC1
IC2
IC3
IC4
DQ0
DQ0
DQ0
DQ0
Drive
I/O Channel

Fig. 3


1
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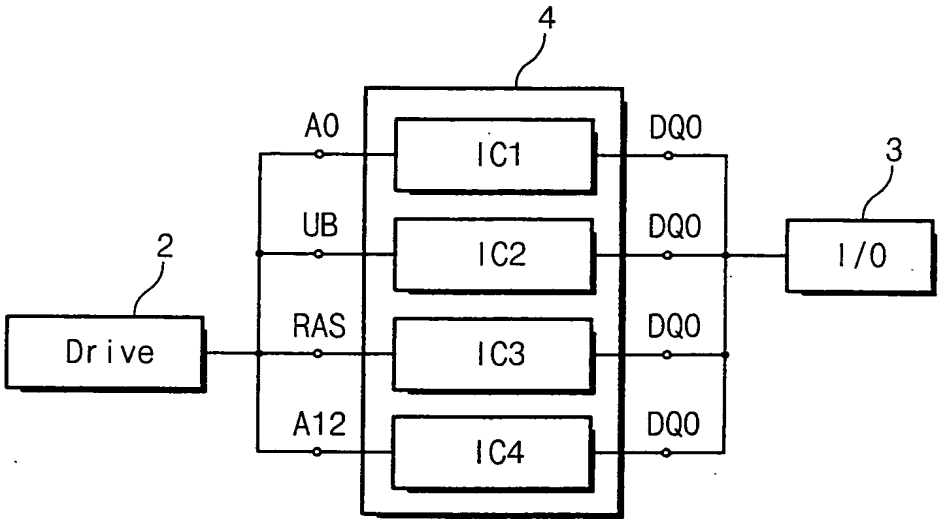
3
Drive
RAS
UB
RAS
IC1
IC2
IC3
DQ0
DQ0
DQ0
I/O

Fig. 4


4
2
3
Drive
A0
UB
RAS
A12
IC1
IC2
IC3
IC4
DQ0
DQ0
DQ0
DQ0
I/O